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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,644	12/27/2001	Katrina Mikhaylichenko	LAM2P316	7982

25920 7590 02/18/2004

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 02/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,644	MIKHAYLICHENKO ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 10th, 2003 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-24) are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) in view of Apelgren et al. (U.S. Patent 6,315,637).

In re claim 1, **AAPA** discloses a method for cleaning a semiconductor wafer, comprising: plasma etching a feature **(FIGS. 1A-B: 17)** into a low K dielectric layer **(FIGS. 1A-B: 16)** having a photoresist mask **(FIG. 1A: 18)**, the plasma generating etch residues **(FIG. 1A: 22)** in and around the feature (page 1, line 20 to page 2, line 17 and **FIGS. 1A-B**); and ashing the semiconductor wafer to remove the photoresist mask, the

ashing generating ashing residues **(FIG. 1B: 27)** (page 2, line 18 to page 3, line 4 and **FIG. 1B**);

AAPA discloses (page 3, lines 5-12) removing the etching residues and the ashing residues from the low K dielectric layer by moving the wafer into the chemical bath containing liquids but does not explicitly disclose removing the etching residues and the ashing residues from the low K dielectric layer having the plasma etched feature, the removing being enhanced by srubbing the low K dielectric layer of the semiconductor wafer with a wet brush that applied a fluid mixture including a cleaning chemistry and a wetting agent.

Apelgren discloses a method for cleaning a semiconductor wafer, comprising (col. 4, line 6 to col. 5, line 51 and **FIGS. 1-7**): plasma etching a feature **(FIGS. 3-4: 28 and 30)** (col. 4, lines 17-28) into a low K dielectric layer **(FIGS. 3-4: 24)** (col. 2, lines 2-15 and col. 4, lines 6-16) having a photoresist mask **(FIG. 4: 26)** (col. 3, line 66 to col. 4, line 5), and removing the etching residues and the ashing residues from the low K dielectric layer having the plasma etched feature, the removing being enhanced by scrubbing the low K dielectric layer of the semiconductor wafer with a wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent (col. 5, lines 24-51). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Apelgren to enable the process of removing the etching residues and the ashing residues of AAPA using the wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent to

be performed and furthermore to remove any remnants of the layer of photoresist (col. 5, lines 25-26).

In re claim 8, **Apelgren** discloses scrubbing the low K dielectric layer using the brush while applying deionized water after removing the etching residues and the ashing residues (col. 5, lines 24-30).

3. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) in view of Apelgren et al. (U.S. Patent 6,315,637) as applied to claims 1 and 8 above, and further in view of Yoon (U.S. Pub. 2002/0090784).

In re claim 2, **Yoon** discloses wherein the wetting agent is a surfactant and the cleaning chemistry includes a combination of NH_2OH, H_2O_2, and deionized (DI) water (page 4, paragraph [0048]).

In re claim 3, the use of a surfactant selected from a group comprising fluorosurfactants and hydrocarbon surfactants is well-known to one of ordinary skill in the art of making semiconductor devices. It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the known process into AAPA and Apelgren's method to enable provision of the surfactant of AAPA and Apelgren's.

In re claims 4 and 5, there is no evidence indicating that the percent by weight range of the surfactant concentration is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05.

In re claims 6 and 7, **Yoon** discloses wherein the combination ratio of NH_2OH, H_2O_2, and deionized (DI) water is between about 1:4:20 (page 4, paragraph [0048]). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA, Apelgren, and Yoon to enable the process of removing the etching residues and the ashing residues of AAPA using the wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent to be performed and furthermore to completely remove the damaged layer and the plate-shaped defect (page 4, paragraph [0048]).

4. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) in view of Apelgren et al. (U.S. Patent 6,315,637).

In re claim 9, **AAPA** discloses a method for cleaning a semiconductor wafer, comprising: plasma etching a feature **(FIGS. 1A-B: 17)** into a low K dielectric layer **(FIGS. 1A-B: 16)**, the plasma generating etch residues **(FIG. 1A: 22)** in and around the feature (page 1, line 20 to page 2, line 17 and **FIGS. 1A-B**); and subjecting the semiconductor wafer to an ashing operation, the ashing operation generating ashing residues **(FIG. 1B: 27)** (page 2, line 18 to page 3, line 4 and **FIG. 1B**);

AAPA discloses (page 3, lines 5-12) removing the etching residues and the ashing residues from the low K dielectric layer by moving the wafer into the chemical bath containing liquids but does not explicitly disclose scrubbing the low K dielectric layer having the plasma-etched feature, using a mixture fluid including a cleaning chemistry and a wetting agent, the wetting agent being configured to condition the low K dielectric

layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry.

Apelgren discloses a method for cleaning a semiconductor wafer, comprising (col. 4, line 6 to col. 5, line 51 and **FIGS. 1-7**): plasma etching a feature **(FIGS. 3-4: 28 and 30)** (col. 4, lines 17-28) into a low K dielectric layer **(FIGS. 3-4: 24)** (col. 2, lines 2-15 and col. 4, lines 6-16) having a photoresist mask **(FIG. 4: 26)** (col. 3, line 66 to col. 4, line 5), and scrubbing the low K dielectric layer having the plasma-etched feature, using a mixture fluid including a cleaning chemistry and a wetting agent, the wetting agent being configured to condition the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry (col. 5, lines 24-51). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Apelgren to enable the process of removing the etching residues and the ashing residues of AAPA using the wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent to be performed and furthermore to remove any remnants of the layer of photoresist (col. 5, lines 25-26).

In re claim 10, **Apelgren** discloses scrubbing the low K dielectric layer using the brush while applying deionized water after removing the etching residues and the ashing residues (col. 5, lines 24-30).

5. Claims 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) in view of Apelgren et al. (U.S. Patent

6,315,637) as applied to claims 9 and 10 above, and further in view of Yoon (U.S. Pub. 2002/0090784).

In re claim 11, **Yoon** discloses wherein the wetting agent is a surfactant and the cleaning chemistry includes a combination of NH_2OH, H_2O_2, and deionized (DI) water (page 4, paragraph [0048]).

In re claim 12, the use of a surfactant selected from a group comprising fluorosurfactants and hydrocarbon surfactants is well-known to one of ordinary skill in the art of making semiconductor devices. It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the known process into AAPA and Apelgren's method to enable provision of the surfactant of AAPA and Apelgren's.

In re claims 13 and 14, there is no evidence indicating that the percent by weight range of the surfactant concentration is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05.

In re claims 15 and 16, **Yoon** discloses wherein the combination ratio of NH_2OH, H_2O_2, and deionized (DI) water is between about 1:4:20 (page 4, paragraph [0048]). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA, Apelgren, and Yoon to enable the process of removing the etching residues and the ashing residues of AAPA using the wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent to be

performed and furthermore to completely remove the damaged layer and the plate-shaped defect (page 4, paragraph [0048]).

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) in view of Apelgren et al. (U.S. Patent 6,315,637).

In re claim 17, **AAPA** discloses a method for cleaning a semiconductor wafer, comprising: plasma etching a feature **(FIGS. 1A-B: 17)** into a low K dielectric layer **(FIGS. 1A-B: 16)**, the plasma generating etch residues **(FIG. 1A-B: 22)** in and around the feature (page 1, line 20 to page 2, line 17 and **FIGS. 1A-B**); and subjecting the semiconductor wafer to an ashing operation, the ashing operation generating ashing residues **(FIG. 1B: 27)** (page 2, line 18 to page 3, line 4 and **FIG. 1B**);

AAPA discloses (page 3, lines 5-12) removing the etching residues and the ashing residues from the low K dielectric layer by moving the wafer into the chemical bath containing liquids but does not explicitly disclose scrubbing the low K dielectric layer having the plasma-etched feature, using a mixture fluid including a cleaning chemistry and a wetting agent, the wetting agent being configured to condition the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry; and scrubbing the low K dielectric layer having the plasma etched feature, using the brush while applying deionized (DI) water after removing the etching residues and the ashing residues.

Apelgren discloses a method for cleaning a semiconductor wafer, comprising (col. 4, line 6 to col. 5, line 51 and **FIGS. 1-7**): plasma etching a feature **(FIGS. 3-4: 28 and 30)** (col. 4, lines 17-28) into a low K dielectric layer **(FIGS. 3-4: 24)** (col. 2, lines 2-

15 and col. 4, lines 6-16) having a photoresist mask **(FIG. 4: 26)** (col. 3, line 66 to col. 4, line 5), and scrubbing the low K dielectric layer having the plasma-etched feature, using a mixture fluid including a cleaning chemistry and a wetting agent, the wetting agent being configured to condition the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry; and scrubbing the low K dielectric layer having the plasma etched feature, using the brush while applying deionized (DI) water after removing the etching residues and the ashing residues (col. 5, lines 24-51). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Apelgren to enable the process of removing the etching residues and the ashing residues of AAPA using the wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent to be performed and furthermore to remove any remnants of the layer of photoresist (col. 5, lines 25-26).

7. Claims 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) in view of Apelgren et al. (U.S. Patent 6,315,637) as applied to claim 17 above, and further in view of Yoon (U.S. Pub. 2002/0090784).

In re claim 18, **Yoon** discloses wherein the wetting agent is a surfactant and the cleaning chemistry includes a combination of NH_2OH, H_2O_2, and deionized (DI) water (page 4, paragraph [0048]).

In re claim 19, the use of a surfactant selected from a group comprising fluorosurfactants and hydrocarbon surfactants is well-known to one of ordinary skill in

the art of making semiconductor devices. It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the known process into AAPA and Apelgren's method to enable provision of the surfactant of AAPA and Apelgren's.

In re claims 20 and 21, there is no evidence indicating that the percent by weight range of the surfactant concentration is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05.

In re claims 22 and 23, **Yoon** discloses wherein the combination ratio of NH_2OH, H_2O_2, and deionized (DI) water is between about 1:4:20 (page 4, paragraph [0048]). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA, Apelgren, and Yoon to enable the process of removing the etching residues and the ashing residues of AAPA using the wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent to be performed and furthermore to completely remove the damaged layer and the plate-shaped defect (page 4, paragraph [0048]).

8. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) in view of Apelgren et al. (U.S. Patent 6,315,637) and Yoon (U.S. Pub. 2002/0090784).

In re claim 17, **AAPA** discloses a method for cleaning a semiconductor wafer, comprising: plasma etching a feature **(FIGS. 1A-B: 17)** into a low K dielectric layer **(FIGS. 1A-B: 16)**, the plasma generating etch residues **(FIG. 1A: 22)** in and around the

feature (page 1, line 20 to page 2, line 17 and **FIGS. 1A-B**); and subjecting the semiconductor wafer to an ashing operation, the ashing operation generating ashing residues **(FIG. 1B: 27)** (page 2, line 18 to page 3, line 4 and **FIG. 1B**);

AAPA discloses (page 3, lines 5-12) removing the etching residues and the ashing residues from the low K dielectric layer by moving the wafer into the chemical bath containing liquids but does not explicitly disclose scrubbing the low K dielectric layer having the plasma-etched feature, using a mixture fluid including a cleaning chemistry and a wetting agent, the wetting agent being configured to condition the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry; and scrubbing the low K dielectric layer having the plasma etched feature, using the brush while applying deionized (DI) water after removing the etching residues and the ashing residues.

Apelgren discloses a method for cleaning a semiconductor wafer, comprising (col. 4, line 6 to col. 5, line 51 and **FIGS. 1-7**): plasma etching a feature **(FIGS. 3-4: 28 and 30)** (col. 4, lines 17-28) into a low K dielectric layer **(FIGS. 3-4: 24)** (col. 2, lines 2-15 and col. 4, lines 6-16) having a photoresist mask **(FIG. 4: 26)** (col. 3, line 66 to col. 4, line 5), and scrubbing the low K dielectric layer having the plasma-etched feature, using a mixture fluid including a cleaning chemistry and a wetting agent, the wetting agent being configured to condition the low K dielectric layer to facilitate cleaning of the etch residues and the ashing residues with the cleaning chemistry; and scrubbing the low K dielectric layer having the plasma etched feature, using the brush while applying deionized (DI) water after removing the etching residues and the ashing residues (col. 5,

lines 24-51). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Apelgren to enable the process of removing the etching residues and the ashing residues of AAPA using the wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent to be performed and furthermore to remove any remnants of the layer of photoresist (col. 5, lines 25-26).

Neither **AAPA** nor **Apelgren** explicitly disclose wherein the wetting agent being a surfactant and the cleaning chemistry being a standard clean-l (SC-1) solution including a combination of NH_2OH, H_2O_2, and deionized (DI) water, the surfactant having a concentration between about 0.005 percent by weight to about 0.1 percent by weight, combination ratio of NH_2OH, H_2O_2, and DI water being between about 1:4:10 and about 1:4:30.

Yoon discloses wherein the wetting agent being a surfactant and the cleaning chemistry being a standard clean-1 (SC-1) including a combination of NH_2OH, H_2O_2, and deionized (DI) water (page 4, paragraph [0048]) wherein the combination ratio of NH_2OH, H_2O_2, and deionized (DI) water is about 1:4:20 (page 4, paragraph [0048]). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA, Apelgren, and Yoon to enable the process of removing the etching residues and the ashing residues of AAPA using the wet brush that applies a fluid mixture including a cleaning chemistry and a wetting agent to be performed and furthermore to completely remove the damaged layer and the plate-shaped defect (page 4, paragraph [0048]).

There is no evidence indicating that the percent by weight range of the surfactant concentration is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05.

Response to Amendment

Response to Arguments

Applicant's arguments filed December 10, 2003 have been fully considered but they are not persuasive.

In response to Applicant's argument that Vyoda et al. does not teach or suggest how to clean post-etch and strip residues from a wafer as recited by Applicants' claims, examiner respectfully disagree. Applicants are directed to pages 2-12 in the present Office Action where the newly discovered reference Apelgren et al. (U.S. Patent 6,315,637) in combination with AAPA and Yoon discloses the Applicants' claims.

For this reason, examiner holds the rejection proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
February 10, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER